IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Gurtej Singh Sandhu et al.	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.676US2
Title:	CHEMICAL VAPOR DEPOSITION OF TITANIUM	

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

When the above-identified patent application is taken up for consideration, please amend the application as follows:

IN THE SPECIFICATION

Please make the paragraph substitutions indicated in the appendix entitled Clean Version of Amended Specification Paragraph. The specific changes incorporated in the substitute paragraph are shown in the following marked-up version of the original paragraph:

The paragraph beginning on page 1, line 4 is amended as follows:

This application is a Divisional of U.S. Application No. 09/489,187, filed on January 20, 2000, which is a continuation-in-part of U.S. Application Serial No. 09/030,705, filed February 25, 1998, now issued as U.S. Patent 6,143,362 on November 7, 2000, which is hereby incorporated by reference in its entirety.

IN THE CLAIMS

Please cancel claims 1-43 and 46-59 after adding the following new claims.

60. (New) An integrated circuit comprising:

a semiconductor substrate;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the

contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

61. (New) The integrated circuit of claim 60, wherein the titanium alloy includes titanium and zinc.

62. (New) The integrated circuit of claim 60, wherein the insulator layer includes silicon dioxide (SiO_2).

63. (New) The integrated circuit of claim 60, wherein the electronic device includes a transistor.

64. (New) An integrated circuit comprising:

a semiconductor substrate;

a transistor formed on the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

65. (New) The integrated circuit of claim 64, wherein the titanium alloy includes titanium and zinc.

66. (New) The integrated circuit of claim 64, wherein the insulator layer includes silicon dioxide (SiO_2).

67. (New) The integrated circuit of claim 64, wherein the contact opening includes a high aspect ratio contact opening.

68. (New) An integrated circuit comprising:

a semiconductor substrate;

an electronic device formed on the semiconductor substrate, the electronic device having an active region;

a borophosphous silicate glass (BPSG) layer over the active region;

an alloy layer of a titanium alloy within a contact opening in the borophosphous silicate glass (BPSG) layer, the contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

69. (New) The integrated circuit of claim 68, wherein the titanium alloy includes titanium and zinc.

70. (New) The integrated circuit of claim 68, wherein the electronic device includes a transistor.

71. (New) The integrated circuit of claim 68, wherein the contact opening includes a high aspect ratio contact opening.

72. (New) An integrated circuit comprising:

a semiconductor substrate;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the active region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

73. (New) The integrated circuit of claim 72, wherein the titanium alloy includes titanium and zinc.

74. (New) The integrated circuit of claim 72, wherein the electronic device includes a transistor.

75. (New) The integrated circuit of claim 72, wherein the insulator layer includes silicon dioxide (SiO_2).

76. (New) The integrated circuit of claim 72, wherein the insulator layer includes borophosphous silicate glass (BPSG).

77. (New) An integrated circuit comprising:

a semiconductor substrate;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

an insulating layer over the source/drain region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the insulating layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

78. (New) The integrated circuit of claim 77, wherein the titanium alloy includes titanium and zinc.

79. (New) The integrated circuit of claim 77, wherein the insulator layer includes silicon dioxide (SiO_2).

80. (New) The integrated circuit of claim 77, wherein the insulator layer includes borophosphous silicate glass (BPSG).

81. (New) An integrated circuit comprising:

a semiconductor substrate;

a transistor coupled to the semiconductor substrate, the transistor having a source/drain region;

a borophosphous silicate glass (BPSG) layer over the source/drain region;

an alloy layer of a titanium alloy within a high aspect ratio contact opening in the borophosphous silicate glass (BPSG) layer, the high aspect ratio contact opening being at least partially over the source/drain region, wherein the titanium alloy comprises titanium and an element selected from the group consisting of zinc, cadmium, mercury, aluminum, gallium, indium, tin, silicon, germanium, lead, arsenic and antimony; and

a titanium silicide contact coupled to the alloy layer.

82. (New) The integrated circuit of claim 81, wherein the titanium alloy includes titanium and zinc.

83. (New) An integrated circuit comprising:

a semiconductor substrate;

an electronic device coupled to the semiconductor substrate, the electronic device having an active region;

an insulating layer over the active region;

an alloy layer of a titanium alloy within a contact opening in the insulating layer, the contact opening being at least partially over the active region, wherein the alloy layer is produced using a method including:

forming a seed layer supported by a substrate by combining a first precursor with a first reducing agent; and

forming the titanium layer supported by the substrate by combining a titanium-containing precursor with the seed layer.

REMARKS

Currently claims 44-45 and 60-83 are pending in the application. The Applicant respectfully requests that the preliminary amendment described herein be entered into the record prior to examination and consideration of the above-identified application. The Examiner is invited to contact Applicant's Representatives at the below-listed telephone number if there are any questions regarding this Preliminary Amendment or if prosecution of this application may be assisted thereby.

Respectfully submitted,

GURTEJ SINGH SANDHU ET AL.

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This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

CLEAN VERSION OF AMENDED SPECIFICATION PARAGRAPHS

CHEMICAL VAPOR DEPOSITION OF TITANIUM
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The paragraph beginning on page 1, line 4.

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